AMENDMENT TO THE CLAIMS

Claim 1 (currently amended): An inductance measurement circuit for measuring an inductance of a wire-loop, said inductance ~~measure~~ measurement circuit comprising:

a pair of ~~resistance-inductance-capacitance~~ driver circuits in electrical communication with a wire-loop;

a demodulation circuit in electrical communication with said pair of ~~resistance-inductance-capacitance~~ driver circuits, said demodulation circuit producing a demodulated signal;

~~a filter in electrical communication with said demodulation circuit, said filter producing a filtered signal;~~ and

~~an analog-to-digital converter~~means for converting an analog signal into a digital signal in electrical communication with said ~~filter~~pair of driver circuits, said ~~analog-to-digital converter~~means for converting an analog signal into a digital signal producing a digitized signal representing an inductance measured ~~on~~ of the wire-loop.

Claim 2 (currently amended): The inductance measurement circuit of Claim 1 further comprising an amplifier circuit in electrical communication between said ~~filter~~ demodulation circuit and said ~~analog-to-digital converter~~means for converting an analog signal into a digital signal, said amplifier producing an amplified signal.

Claim 3 (currently amended): The inductance measurement circuit of Claim 1 further comprising a pre-amplifier circuit in electrical communication between said pair of ~~resistance-inductance-capacitance~~ driver circuits and said demodulation circuit.

Claim 4 (currently amended): The inductance measurement circuit of Claim 1 wherein said pair of ~~resistance-inductance-capacitance~~ driver circuits operate at a fixed-frequency.

Claim 5 (currently amended): The inductance measurement circuit of Claim 1 wherein said demodulation circuit includes a demodulation oscillator, said demodulation circuit producing an output derived from said pair of ~~resistance-inductance-capacitance~~ driver circuits and said demodulation oscillator.

Claim 6 (currently amended): The inductance measurement circuit of Claim ~~5~~5 wherein said output is a demodulated signal substantially corresponding to an envelope of the combined RLC waveform.

Claim 7 (currently amended): The inductance measurement circuit of Claim 1 ~~wherein said filter is a bandpass~~ further comprising a filter which removes noise substantially outside a ~~baseband~~ selected frequency range of the inductance measurement circuit, said filter in communication between said demodulation circuit and said means for converting an analog signal into a digital signal.

Claim 8 (original): The inductance measurement circuit of Claim 1 wherein said demodulation circuit is a synchronous demodulator.

Claim 9 (original): The inductance measurement circuit of Claim ~~8~~8 wherein said synchronous demodulator includes a plurality of analog switches.

Claim 10 (currently amended): The inductance measurement circuit of Claim ~~8~~8 wherein said demodulation circuit and said pair of ~~resistance-inductance-capacitance~~ driver circuits operate at substantially ~~similar frequencies~~the same frequency.

Claim 11 (currently amended): The inductance measurement circuit of Claim 1 further comprising a dc voltage offset generator for producing a dc offset voltage and a signal conditioning circuit in electrical communication between said ~~filter~~ demodulation circuit and said dc voltage offset generator, said signal conditioning circuit removing said dc voltage from said ~~filtered~~ demodulated signal thereby allowing said ~~filtered~~ demodulated signal to be amplified without saturating.

Claim 12 (currently am nded): The inductance measurement circuit of Claim 1 wherein said pair of ~~resistance-inductance-capacitance~~ driver circuits include a pair of resistance-capacitance networks, each of said pair of resistance-capacitance networks driven by a multi-state buffer, each of said pair of resistance-capacitance networks having a resistance.

Claim 13 (original): The inductance measurement circuit of Claim 12~~12~~ wherein each of said pair of resistance-capacitance networks has a large apparent impedance.

Claim 14 (original): The inductance measurement circuit of Claim 12~~12~~ wherein each of said pair of resistance-capacitance networks is balanced using said multi-state buffer to modulate said resistance.

Claim 15 (original): The inductance measurement circuit of Claim 14~~14~~ wherein said multi-state buffer is driven at a high rate compared to a desired sinusoidal frequency by a duty cycle controlled voltage.

Claim 16 (currently amended): The inductance measurement circuit of Claim 1 wherein the wire-loop is directly coupled to said pair of ~~resistance-inductance-capacitance~~ driver circuits.

Claim 17 (currently amended): The inductance measurement circuit of Claim 1 further comprising a transformer coupling the wire-loop to said pair of ~~resistance-inductance-capacitance~~ driver circuits, said transformer rejecting a common-mode noise originating from the wire-loop.

Claim 18 (currently amended): The inductance measurement circuit of Claim 1 wherein said ~~analog-to-digital converter~~means for converting an analog signal into a digital signal is a delta-sigma analog-to-digital converter.

Claim 19 (currently am nded): The inductance measurement circuit of Claim 1 wherein said pair of ~~resistance-inductance-capacitance~~ driver circuits is driven by a differential, periodic waveform.

Claim 20 (original): The inductance measurement circuit of Claim 19~~19~~ wherein said periodic waveform is a sine wave.

Claim 21 (currently amended): The inductance measurement circuit of Claim 19~~19~~ wherein said periodic waveform is substantially a square wave, said square wave having a frequency substantially similar to an operating frequency of said pair of ~~resistance-inductance-capacitance~~ driver circuits.

Claim 22 (original): The inductance measurement circuit of Claim 1 wherein said dc offset generator includes a digital-to-analog converter.

Claim 23 (original): The inductance measurement circuit of Claim 1 wherein said dc offset generator uses pulse width modulation to adjust a duty cycle of a square wave.

Claim 24 (currently amended): The inductance measurement circuit of Claim 1 wherein said ~~analog-to-digital converter~~means for converting an analog signal into a digital signal includes a voltage reference input, said inductance measurement circuit further comprising a signal generator connected to said voltage reference input, an output of said signal generator selected to match a characteristic of internal noise in said inductance measurement circuit.

Claim 25 (original): The inductance measurement circuit of Claim 1 wherein a plurality of said inductance measurement circuits are operating in close proximity, each of said plurality of said inductance measurement circuits operating at a unique carrier frequency and in a distinct frequency band from other closely proximate said inductance measurement circuits.

Claim 26 (original): The inductance measurement circuit of Claim 25~~25~~ wherein each said carrier frequency is separated from each said carrier frequency of a proximate said inductive measurement circuit to provide sufficient bandwidth for operation.

Claim 27 (original): The inductance measurement circuit of Claim 25~~25~~ wherein each said carrier frequency is separated from each other said carrier frequency by between approximately 50 to approximately 1200 Hertz.

Claim 28 (original): The inductance measurement circuit of Claim 1 wherein said demodulation circuit is a full-wave bridge rectifier.

Claim 29 (currently amended): The inductance measurement circuit of Claim 1 further comprising a heating element in close proximity to a capacitor of said pair of ~~resistance-inductance-capacitance~~ driver circuits.

Claim 30 (original): The inductance measurement circuit of Claim 29~~29~~ wherein said heating element is thermally coupled to said capacitor.

Claim 31 (original): The inductance measurement circuit of Claim 29~~29~~ wherein said heating element is a resistor connected to a variable current source.

Claim 32 (original): The inductance measurement circuit of Claim 31~~31~~ wherein said resistor and said capacitor are thermally insulated to improve thermal efficiency.

Claim 33 (currently amended): The inductance measurement circuit of Claim 1 wherein said ~~analog-to-digital-converter~~means for converting an analog signal into a digital signal includes a low-pass filter.

Claim 34 (currently amended): The inductance measurement circuit of Claim 1 wherein said ~~analog-to-digital-converter~~means for converting an analog signal into a digital signal includes differential inputs and rejects a common-mode

noise ~~originating from~~applied to said inductance measurement circuit by the wire-loop.

Claim 35 (currently amended): The inductance measurement circuit of Claim 1 wherein a characteristic of ~~each~~ at least one said pair of ~~resistance-inductance-capacitance~~ driver circuits is modulated to balance said pair of ~~resistance-inductance-capacitance~~ driver circuits for common-mode noise rejection.

Claim 36 (new): An inductance measurement circuit for measuring an inductance of a wire-loop, said inductance measurement circuit comprising:

a pair of driver circuits in electrical communication with a wire-loop;

a demodulation circuit in electrical communication with said pair of resistance-inductance-capacitance driver circuits, said demodulation circuit producing a demodulated signal; and

a filter in electrical communication with said demodulation circuit, said filter producing a filtered signal.

Claim 37 (new): An inductance measurement circuit for measuring an inductance of a wire-loop, said inductance measurement circuit comprising:

a pair of driver circuits in electrical communication with a wire-loop;

a demodulation circuit in electrical communication with said pair of driver circuits, said demodulation circuit producing a demodulated signal;

a filter in electrical communication with said demodulation circuit, said filter producing a filtered signal; and

an analog-to-digital converter converting an analog signal into a digital signal in electrical communication with said filter, said analog-to-digital converter producing a digitized signal representing an inductance measured of the wire-loop.

Claim 38 (new): An inductance measurement circuit for measuring an inductance of a wire-loop, said inductance measurement circuit comprising:

a pair of driver circuits in electrical communication with a wire-loop;

a demodulation circuit in electrical communication with said pair of resistance-inductance-capacitance driver circuits, said demodulation circuit producing a demodulated signal; and

an analog-to-digital converter converting an analog signal into a digital signal in electrical communication with said demodulation circuit, said analog-to-digital converter producing a digitized signal representing an inductance measured of the wire-loop.